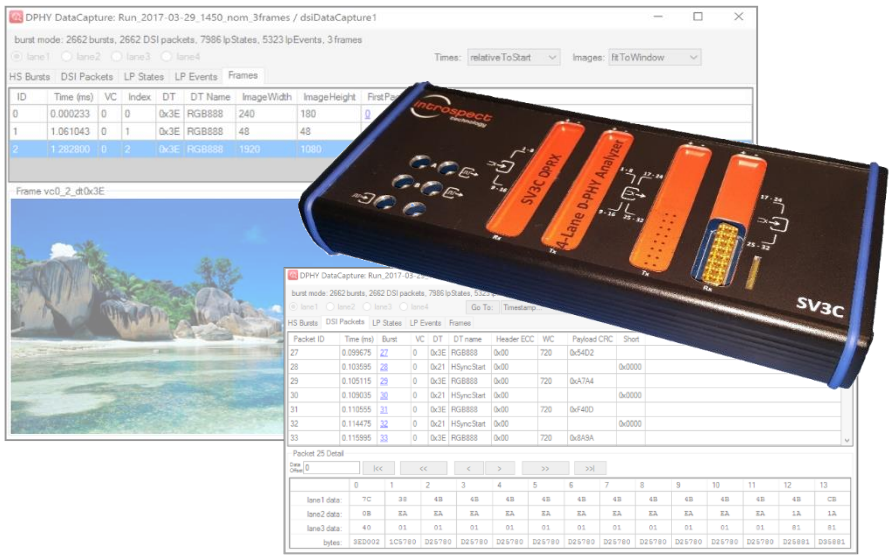
SV3C DPRX MIPI D-PHY Analyzer



Data Sheet

Ordering Information:

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Introduction

Overview

The SV3C-DPRX D-PHY Analyzer is an ultra-portable, high-performance instrument for exercising and validating MIPI D-PHY transmitters as well as probing live MIPI D-PHY links. The Analyzer is data-rate agile, making it ideal for the capture and analysis of MIPI transmitters used in cameras, displays, and other devices. It also includes integrated LP and HS receivers, dynamic termination, and offers sophisticated capture, compare, and analysis modes.

The D-PHY Analyzer operates using the highly versatile Introspect ESP software environment that allows for automating transmitter tests such as CRC error counting or protocol timings.

This document includes electrical specifications of the Analyzer and provides details on the various methods for the capture and analysis of D-PHY traffic.

Please refer to the ***Help Menu*** within the Introspect ESP software for additional operating instructions.

Key Benefits

- Any-rate operation
- Flexible lane assignment
- Protocol Analyzer suite for CSI-2, DSI, and DSI-2
- Video frame extraction
- Precision time stamps to help understand each physical layer event
- Advanced triggering based on physical-layer or protocol-layer events
- Continuous monitoring mode for long-term error checking
- Programmable trigger I/O
- Intuitive state-of-the-art Python programming environment
- Reconfigurable, protocol customization (on request)

Applications

- Physical layer validation of MIPI D-PHY transmitters
- Protocol analysis for CSI-2, DSI, and DSI-2
- IP and software validation testing
- Debug of active D-PHY links
- Interface test
- Plug-and-play system-level validation

Ordering Information

This product is part of the SV3C family of MIPI analyzer products. The following table describes the part numbers and key feature differentiators.

Table 1 Ordering part numbers for this product and related ones.

Part Number	Name	Key Differentiators
4585	**SV3C-DPRX - SV3C D-PHY Analyzer Bundle (this product)**	Covers the MIPI D-PHY physical layer
4590	**SV3C-DPRXCPRX - SV3C Combo C-PHY/D-PHY Analyzer Bundle**	Combo D-PHY and C-PHY capability
4594	**SV3C DPRX Upgrade**	Firmware and software license upgrade from 4585 to 4590

Features

Complete D-PHY Receiver Implementation

The SV3C DPRX is a complete, integrated, 4-lane D-PHY receiver providing the analog front-end circuitry for D-PHY as well as a complete protocol back-end. As shown in Figure 1, each lane contains low power (LP) threshold voltage detectors, dynamically controlled D-PHY termination resistors, and fully differential high speed (HS) receivers. The real-time behavior of the DPRX enables broad acquisition capabilities on physical-layer and protocol-layer events as detailed in Figure 2. The figure illustrates two common setups for deploying the DPRX, which can be used as either a terminating receiver or to probe live links.

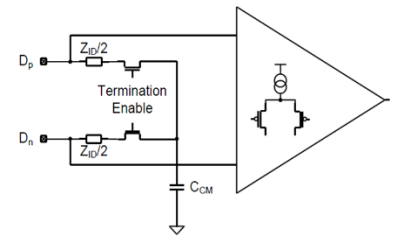

Figure 1 SV3C receiver illustration showing automatic termination switches.

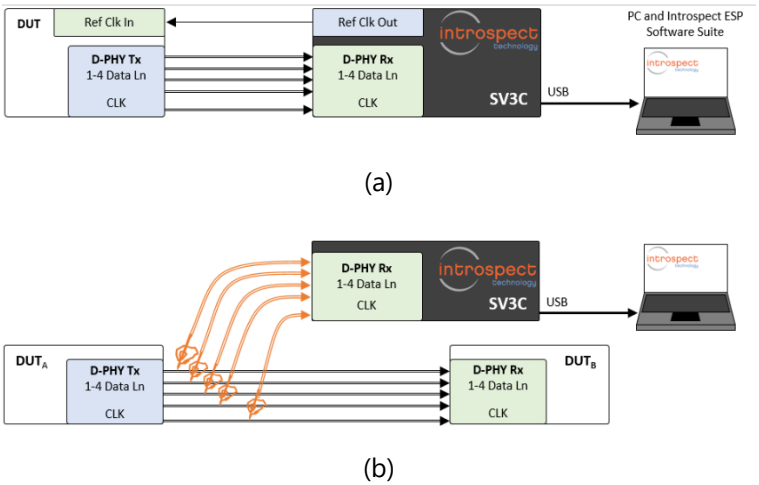

Figure 2 (a) Illustration of the DPRX as a terminating end-point receiver, or (b) while probing a complete D-PHY link.

Protocol Analysis and Precision Time Stamps

The SV3C DPRX is a complete protocol analyzer for both camera and display serial interfaces. Either protocol can be selected within a single session, and the analyzer automatically adjusts its viewer displays based on the protocol being measured (Figure 3). At the same time, irrespective of the protocol, five viewers provide insight into PHY and protocol events while hyperlinks make for quick and intuitive navigation across the layers, namely:

HS Bursts – View each high-speed burst, by lane, with quick statistics of the time of arrival in nanoseconds, SOT offset and captured bits in each

CSI/DSI Packets – Merged traffic from all lanes is shown as unique packets. Headers are decoded for easy, high-level viewing, and errors (CRC, ECC1, ECC2) are automatically highlighted

LP States – Each LP state is captured along with its time of arrival and duration; this viewer is extremely effective for building an visualization of the physical layer events

Frame Viewer – Images are automatically reconstructed, even if incomplete, with details such as pixel format, virtual channel, and image dimensions

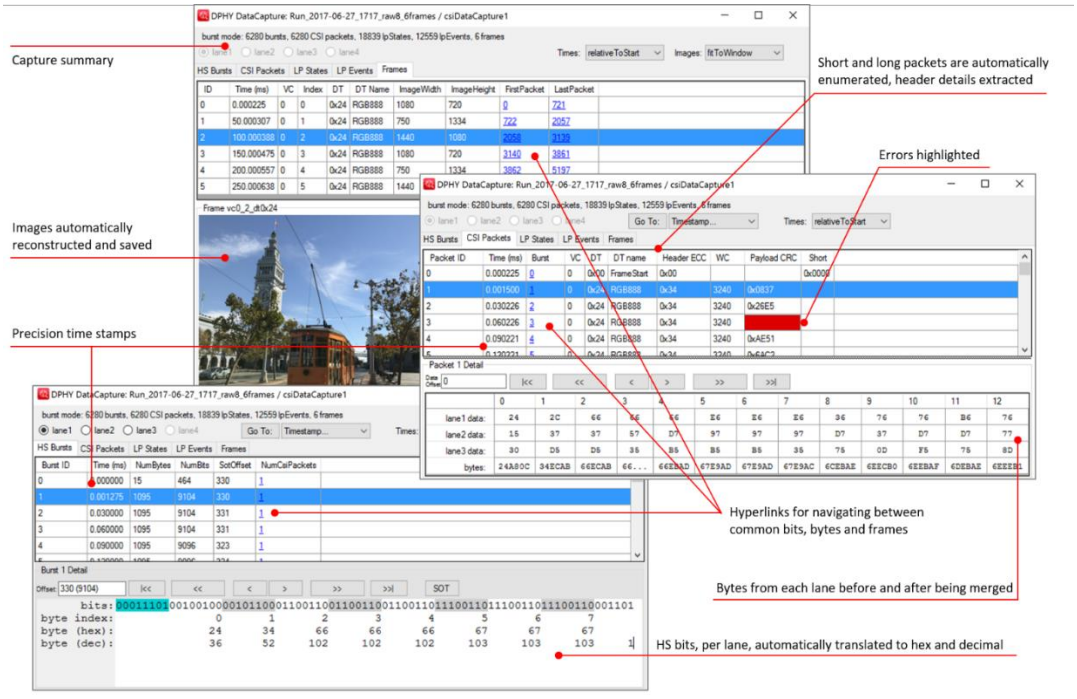

Figure 3 Protocol analyzer views.

To enable the acquisition of high definition video streams under realistic traffic conditions, the SV3C DPRX relies on event-based captures, assigning a time stamp to each pertinent event of the physical layer and protocol layer. This allows for optimized data storage and extremely efficient long-term data analysis. In terms of display, each viewer contains a column dedicated to the precision time stamps of a given burst, packet, LP event or frame. Correlating events in time makes it easy to identify anomalous transitions, unexpected short- or long-packets, and other physical layer perturbations, as depicted in Figure 3.

Hardware CRC Checking and Packet Error Rate Testing

Another fundamental feature of the SV3C-DPRX D-PHY Analyzer is hardware-based packet error-rate detector. Similar to traditional BER, the PERT enables the measurement of real D-PHY transmissions from CSI generators or DSI generators. As illustrated in Figure 4, the Analyzer detects and filters all signal waveforms and compares only the packet data transmitted between SOT and EOT, registering errors after the data has been merged between lanes, thereby comparing errors in packets rather than bits.

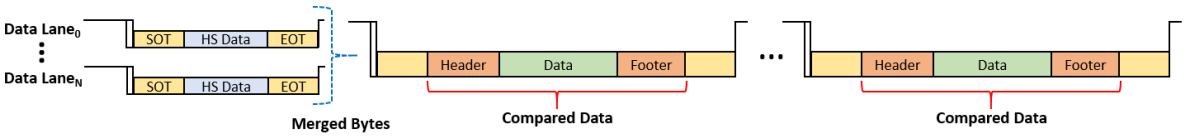

Figure 4 Illustration of packet error rate testing.

Advanced Trigger Modes

Figure 5 shows the user interface for defining the trigger mechanisms within the Analyzer. At the highest level, the Analyzer can be programmed to perform immediate captures (in which all data is measured irrespective of whether there are LP transitions or not) or burst-mode captures (Figure 6). The benefit of the immediate capture mode is that it allows for pattern learning and detecting multiple non-deterministic / non-repetitive packets. On the other hand, triggered captures offer a more focused view of D-PHY global timing parameters. In this mode, the D-PHY Analyzer sets the termination resistors into automatic mode. Then, the analyzer waits for a valid LP to HS entry sequence before enabling a capture. If no valid HS-entry transition is detected, the capture returns an empty array. However, when a valid HS-entry transition is detected, the capture starts immediately.

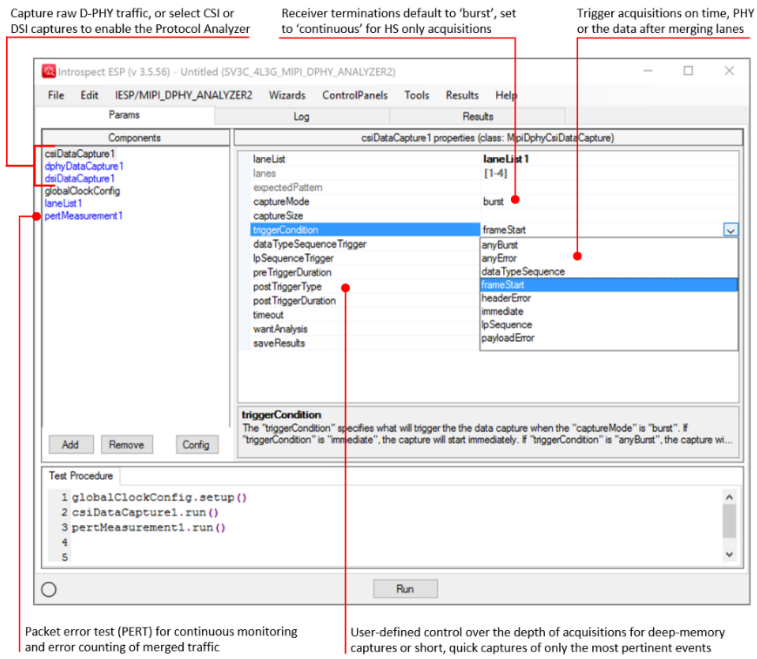

Figure 5 Introspect ESP GUI for the SV3C DPRX. Top left: Components, shows CSI, DSI and PHY data acquisition methods. Top right: Properties, showing CSI Data capture. Bottom: test procedure ready to execute a CSI Data Capture, then PERT.

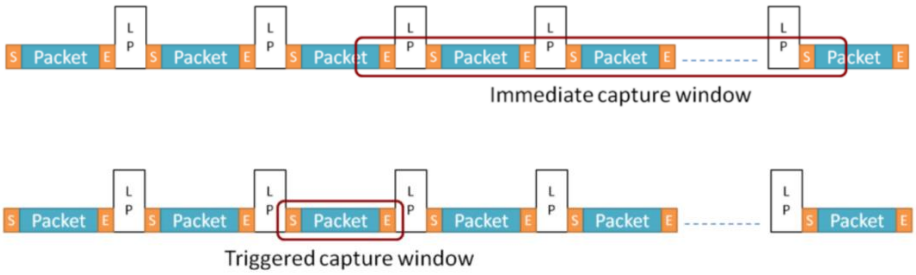

Figure 6 Illustration of multi-packet, per-lane PHY-level capture (Top), and triggered packet capture (Bottom).

Acquisitions and their depth are defined in time, by PHY events or by bytes of merged high-speed traffic. Figure 7 illustrates two methods of triggering acquisitions by PHY events. In Figure 7 (top), an acquisition begins on the first high-speed burst witnessed and completed after user-defined *N* bursts are recorded. In Figure 7 (bottom), a capture begins immediately and the Analyzer records for a user-defined period of *N* nanoseconds. Figure 8 illustrates three examples of triggering acquisitions on merged, high-speed data. The DPRX supports one to four data lanes and independently merges and monitors bytes. Acquisition start is user-defined as the first event observed: (a) error within a

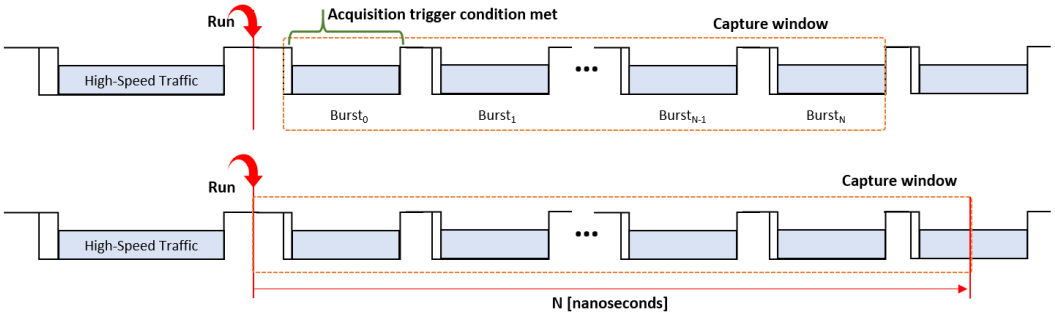

Figure 7 Illustration of two PHY-based acquisitions. Above, recording is triggered on first observed burst and depth is determined by user-defined N bursts. Below, acquisition begins immediately and depth is for a user-defined period of N nanoseconds.

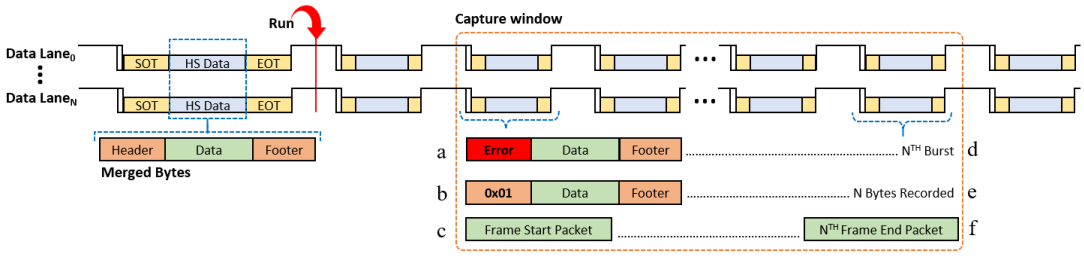

Figure 8 Illustration of three acquisitions triggered on merged high-speed traffic events: (a) header error, (b) user-defined data type identifier and (c) frame start packet. Three methods of acquisition depth are shown: (d) user-defined N bursts, (e) bytes, and (f) frames.

packet header, (b) variable data type identifier, here chosen as 0x01 and (c) frame start packet (CSI only). The depth of the acquisition for each is arbitrarily chosen according to the number of *N* received: (d) bursts, (e) bytes and (f) frame end packets. Finally, for completeness, Table 2 and Table 3 provide a list of trigger mechanism that are available in the Analyzer.

Table 2 DPRX methods for triggering a D-PHY acquisition.

triggerCondition	Type	Trigger Description
anyBurst	PHY	the first high-speed burst witnessed over any data or clock lane
immediate	Time-base	time-base acquisition, beginning immediately when run
lpSequence	PHY	user-defined sequence of LP states, e.g. “11,01,00” reflects a proper LP-HS entry sequence
anyError	CSI, DSI	the first error is registered: header, CRC or payload
dataTypeSequence	CSI, DSI	user-defined integer value to be identified in a packet header
headerError	CSI, DSI	protocol layer, the first error recognized in a packet header
payloadError	CSI, DSI	protocol layer, the first error recognized in a packet payload
frameStart	CSI	CSI-only, any packet with header data type 0x00 indicating the beginning of a frame
verticalSyncStart	DSI	DSI-only, any packet with header data type 0x01 indicating the beginning of a frame

Table 3 Units available for defining depth of an acquisition, accompanied with a user-defined value.

postTriggerType	Type	Description
durationInNs	Time-base	time-base acquisition, defined in nanoseconds
numberOfBursts	PHY	the total number of unique bursts acquired, across all data lanes
numberOfBytes	PHY	the total number of bytes recorded between SOT and EOT of all bursts
numberOfLpCommands	PHY	the first error is registered: header, CRC or payload
numberOfLpStates	PHY	number of unique LP states, e.g. “11,01,00” would be 3
nuberOfFrameEnds	CSI	protocol layer, the number of frame-end packets recorded
numberOfVerticalSyncStarts	DSI	protocol layer, the number of packets with data type identifier 0x01

Automation

The SV3C DPRX D-PHY Analyzer is operated using the award-winning Introspect ESP software, a Python-based scripting environment. Shown in Figure 9, it includes a comprehensive suite of components and methods for executing capture and analysis of D-PHY transmissions, and a canvas for automating test procedures and rich analysis. The Python library is open, and an optional .NET DLL library provides access for integration with DUTs, other test equipment using Python, or alternative programming languages.

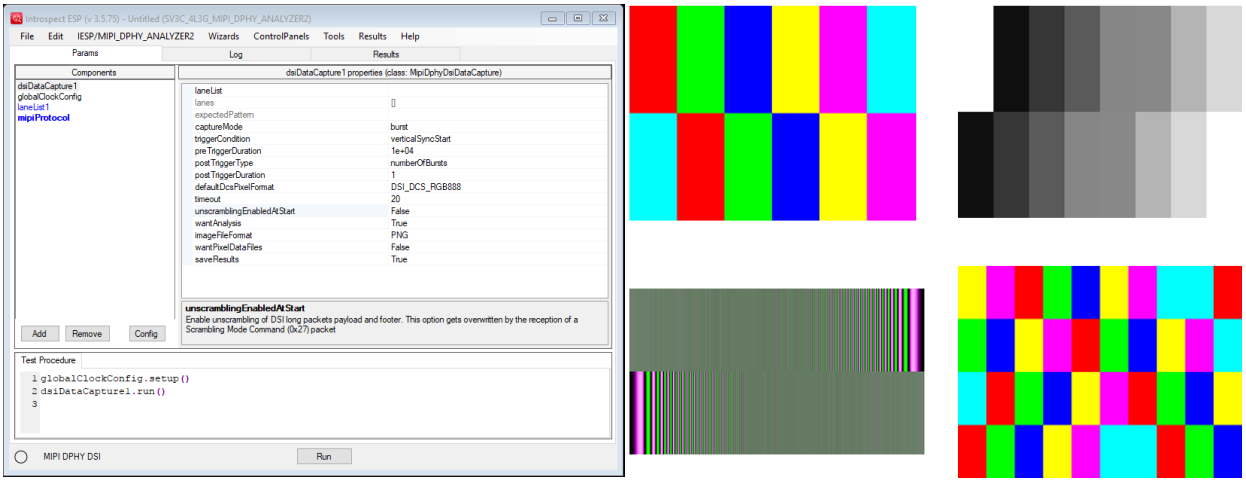

Figure 9 Introspect ESP software environment, left, and right, examples of image captures.

Physical Description and Pinout

Figure 10 shows the physical connections of the SV3C MIPI D-PHY Analyzer. A single HUBER+SUHNER MXP connection provides input for the high-speed D-PHY lanes: four data lanes and one clock (MXP to SMA-Female breakout cable included). Differential SMP connections for reference clock output and input are available for synchronization with devices under test (DUT). A 240-pin SEARAY connection, depicted in Figure 11, provides programmable GPIO for various purposes such as:

- Low-speed communications with DUT via SPI or I2C
- Programmable trigger outputs based on real-time events such as errors, bursts or received data patterns
- Trigger input for data acquisition

Finally, Table 4 shows the pin mapping on the MXP connector.

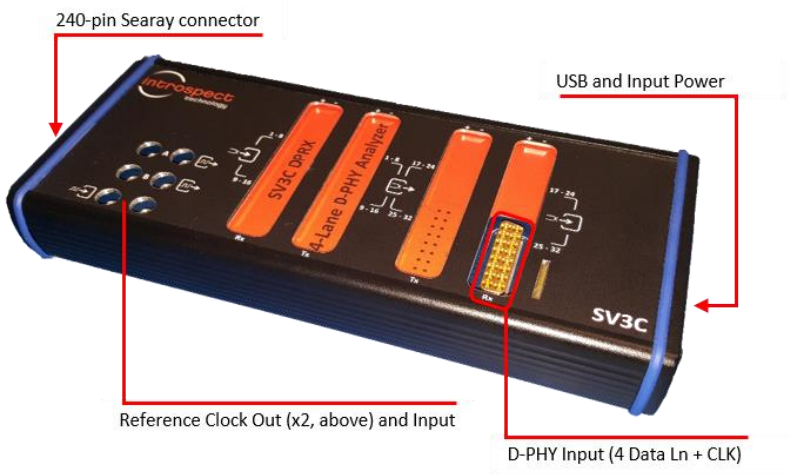

Figure 10 SV3C MIPI D-PHY Analyzer connections.

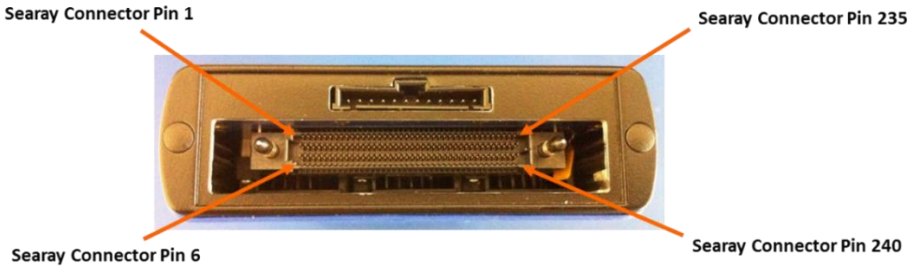

Figure 11 Illustration of the 240-pin SEARAY connector.

Table 4 Mapping of Lower MXP Connector (Lane Pinout).

	Connector Pin Number	Corresponding RX Lane
	1,2	Lane 1 (P,N)
	3,4	Lane 2 (P,N)
	5,6	Lane 3 (P,N)
	9,10	Lane 4 (P,N)
	13, 14	CLK (P,N)

Specifications

Table 5 General Specifications

Parameter	Value	Units	Description and Conditions
Application / Protocol Support			
Physical layer interface	D-PHY		Version 1.2, 2.0
MIPI protocol	CSI-2		Version 1.3, 2.0
	DSI		Version 1.3
	DSI-2		Version 1.0
	Custom		
Compression protocol	VESA		Version 1.2
LP/HS Handling	Automatic		Tester automatically detects LP and HS data
	LP Only		Acquire transitions only between LP wire states
	HS Only		Continuous, high-speed only acquisition
Ports			
Number of Receiver Lanes	4 Data + 1 Clock		
Number of Dedicated Clock Outputs	2		Separate clock for providing reference to the DUT
Number of Dedicated Clock Inputs	1		Used as external Reference Clock input
Number of Trigger Input Pins	3		Armed in software to trigger the start of specific measurements
Number of Flag Output Pins	3		Armed in software to flag test completion or pass/fail criteria
Data Rates and Frequencies			
Minimum Data Rate	80	Mbps	
Maximum Data Rate	3	Gbps	
Minimum External Input Clock Frequency	10	MHz	
Maximum External Input Clock Frequency	250	MHz	
Minimum Output Clock Frequency	10	MHz	
Maximum Output Clock Frequency	250	MHz	
Output Clock Frequency Resolution	1	kHz	
Supported External Input Clock I/O Standards			Support for LVDS, LVPECL, CML, HCSL, and CMOS.
Minimum LP State Period	25	ns	

Table 6 Receiver Characteristics

Parameter	Value	Units	Description and Conditions
Input Coupling			
Input Impedance	50 Hi-Z	Ω Ω	
HS Performance			
Minimum Detectable Differential Voltage	90	mV	
Maximum Allowable Differential Voltage	600	mV	
Resolution Enhancement & Equalization			
Minimum DC Gain	0	dB	
Maximum DC Gain	8	dB	
DC Gain Control	Per-receiver		
Equalization Control	Per-receiver		
Timing Generator Performance			
Resolution at Maximum Data Rate	7.8125	mUI	
Differential Non-Linearity Error	+/- 0.5	LSB	
Integral Non-Linearity Error	+/- 5	ps	
Range	+/- 2	UI	
LP Voltage Threshold Controls			
Minimum Programmable Threshold Voltage	-100	mV	
Maximum Programmable Threshold Voltage	1500	mV	
Threshold Voltage Resolution	1	mV	
Threshold Voltage Accuracy	Larger of 5.0 mV or 2.0 % of programmed value		

Table 7 Clocking Characteristics

Parameter	Value	Units	Description and Conditions
Internal Time Base			
Number of Internal Frequency References	1		
Frequency Resolution of Programmed Data Rate	1	Kbps	

Table 8 Pattern and Protocol Handling Characteristics

Parameter	Value	Units	Description and Conditions
Preset Patterns			
Standard Built-In Patterns	All Zeros		
	D21.5		
	K28.5		
	K28.7		
	DIV.16		
	DIV.20		
	DIV.40		
	DIV.50		
	PRBS.5		
	PRBS.7		
	PRBS.9		
	PRBS.11		
	PRBS.13		
	PRBS.15		
	PRBS.18		
	PRBS.23		
	PRBS.31		
User-programmable Pattern Memory			
Individual Expected Pattern	Per-lane		
Minimum Pattern Segment Size	8	bits	
Total Memory Space for Expected Patterns	4G	Bytes	
BERT Characteristics			
Maximum Packet Size	$2^{32} - 1$		
Maximum Number of Packets	$2^{32} - 1$		
Maximum Number of Repeats	$2^{32} - 1$		
Maximum Time Between SOT in Burst Mode	1	ms	
Minimum Time Between SOT in Burst Mode	TBD	UI	
Capture Memory Depth	4G	Bytes	
Additional Protocol Characteristics			
Escape Mode Command Detection	Per Lane		
De-scrambling	Auto response		Automatically respond to Scrambling Mode Command (0x27) packet
	Manual override		Manually disable scrambling through software
Decompression	Auto PPS		Automatically receive PPS table from transmitter
	Set PPS		Program the PPS table in software

Table 9 Physical Characteristics

Parameter	Value	Units	Description and Conditions
Dimensions			
Length	9.50, 241.30	in, mm	
Width	4.25, 107.95	in, mm	
Height	1.30, 33.30	in, mm	
Weight	2	lb	
Physical Connections			
D-PHY Rx	Huber & Suhner 16-pin MXP		
GPIO	Samtec SEARAY		PN CON-SAMTEC-SEAF-40-01-L-06-2-RA-LP-TR
Ref Clock In	SMP Differential Pair		
Ref Clock Out	SMP Differential Pair		
PC Connection	USB		
Power Switch/Connector	AC adapter provided		110/220 V, 50/60 Hz
Energy Use			
Power Dissipation	< 60	W	

Revision Number	History	Date
1.0	Import from CPRX v1.1.	June 7, 2014
1.1	Updated document template.	June 3, 2015
1.2	Updates to Protocol Analyzer	July 6, 2017
1.3	Updates to text	August 24, 2017

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